IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., a Delaware corporation, Plaintiff, v. FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC., a Delaware corporation, and FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation, Defendants.	C.A. No. 04-1371 (JJF) **REDACTED PUBLIC VERSION**

DECLARATION OF GABRIEL M. RAMSEY IN SUPPORT OF FAIRCHILD'S SUPPLEMENTAL BRIEF IN SUPPORT OF DEFENDANTS' REQUEST TO USE ELEVEN PRIOR ART REFERENCES DURING THE INVALIDITY PHASE OF TRIAL

I, Gabriel M. Ramsey, the undersigned, declare as follows:

1. I am an attorney with the firm of Orrick, Herrington & Sutcliffe LLP, counsel of record for Defendants Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corp. (collectively, "Fairchild"). I am admitted to the Bar of the State of California. I make this declaration in support of Fairchild's Opposition To Plaintiff's Cross-Motion Re: Fairchild's Prior Art Documents And Contentions At Trial. I make this declaration of my own personal knowledge and, if called as a witness, I could and would testify competently to the truth of the matters set forth herein.

2. Attached hereto as Exhibit 1 is a true and correct copy of the January 9, 2006 **REDACTED**

3. Attached hereto as Exhibit 2 is a true and correct copy of Plaintiff's Trial Exhibit List.

4. Attached hereto as Exhibit 3 is a true and correct copy of I REDACTED

5. Attached hereto as Exhibit 4 is a true and correct copy of REDACTED

6. Attached hereto as Exhibit 5 is a true and correct copy of excerpts of REDACTED

7. Attached hereto as Exhibit 6 is a true and correct copy of REDACTED

8. Attached hereto as Exhibit 7 is a true and correct copy of REDACTED

9. Attached hereto as Exhibit 8 is a true and correct copy of REDACTED

10. Attached hereto as Exhibit 9 is a true and correct copy of U.S. Pat. No. 4,823,173.

11. Attached hereto as Exhibit 10 is a true and correct copy of REDACTED

12. Attached hereto as Exhibit 11 is a true and correct copy of REDACTED

13. Attached hereto as Exhibit 12 is a true and correct copy of REDACTED

14. Attached hereto as Exhibit 13 is a true and correct copy of REDACTED

15. Attached hereto as Exhibit 14 is a true and correct copy of REDACTED

16. Attached hereto as Exhibit 15 is a true and correct copy of REDACTED

17. Attached hereto as Exhibit 16 is a true and correct copy of the REDACTED

18. Attached hereto as Exhibit 17 is a true and correct copy of REDACTED

19. Attached hereto as Exhibit 18 is a true and correct copy of REDACTED

20. Attached hereto as Exhibit 19 is a true and correct copy of the claim chart from REDACTED

21. Attached hereto as Exhibit 20 is a true and correct copy of REDACTED

22. Attached hereto as Exhibit 21 is a true and correct copy of the REDACTED

23. Attached hereto as Exhibit 22 is a picture of Defendants' REDACTED

24. Attached hereto as Exhibit 23 is a true and correct copy of

25. Attached hereto as Exhibit 24 is a picture of REDACTED

26. Attached hereto as Exhibit 25 is a true and correct copy of

27. Attached hereto as Exhibit 26 is a true and correct copy of REDACTED

28. Attached hereto as Exhibit 27 is a true and correct copy of the REDACTED

29. Attached hereto as Exhibit 28 is a true and correct copy of the REDACTED

30. Attached hereto as Exhibit 29 is a true and correct copy of the REDACTED

31. Attached hereto as Exhibit 30 is a true and correct copy of the REDACTED

32. Attached hereto as Exhibit 31 is a true and correct copy of the REDACTED

33. Attached hereto as Exhibit 32 is a true and correct copy of the REDACTED

34. Attached hereto as Exhibit 33 is a true and correct copy of the REDACTED

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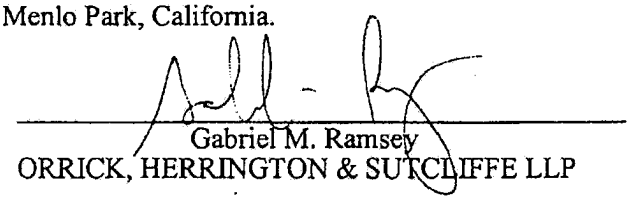
35. Attached hereto as Exhibit 34 is a true and correct copy of the REDACTED

36. Attached hereto as Exhibit 35 is a true and correct copy of the REDACTED

I declare the foregoing is true and correct under penalty of perjury under the laws of the United States of America.

Executed on November 21, 2006 in Menlo Park, California.



Gabriel M. Ramsey
ORRICK, HERRINGTON & SUTCLIFFE LLP

OHS West:260130570.1

EXHIBIT 1

REDACTED IN ITS ENTIRETY

EXHIBIT 2

Exhibit 6 to the Proposed Pretrial Order

UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC.

V.

FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC., and FAIRCHILD SEMICONDUCTOR CORPORATION

POWER INTEGRATIONS' EXHIBIT LIST

C.A. No. 04-1371-JJF

Power Integrations, Inc. reserves the right to supplement or otherwise amend this exhibit list.

PRESIDING JUDGE	PLAINTIFF'S ATTORNEYS	DEFENDANT'S ATTORNEYS
Joseph J. Farnan, Jr.	**William J. Marsden, Jr., Frank E. Scherkenbach, Howard G. Pollack, Michael R. Headley**	**G. Hopkins Guy, III, Vickie L. Feeman, Bas de Blank, Brian H. VanderZanden**
TRIAL DATE (S)	COURT REPORTER	COURTROOM DEPUTY
October 2, 2006	**Leonard Dibbs**	**Anita Bolton**

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
1	U.S. Patent No. 6,249,876 (Balakrishnan *et al.*) with certificate of correction		06/19/01	PIF 00320 – 00333	Balakrishnan	N
2	U.S. Patent No. 6,107,851 (Balakrishnan *et al.*)		08/22/00	PIF 00082 – 00099	Balakrishnan	N
3	U.S. Patent No. 6,229,366 (Balakrishnan *et al.*)		05/08/01	PIF 00217 – 00234	Balakrishnan	N
4	U.S. Patent No. 4,811,075 (Eklund)		03/07/89	PIF 00002 – 00008	Eklund	N
5	File History for U.S. Patent 6,249,876, Serial No. 09/192,959			PIF 00317 – 00408	Balakrishnan	
6	File History for U.S. Patent 6,107,851, Serial No. 09/080,774			PIF 00077 – 00211	Balakrishnan	
7	File History for U.S. Patent 6,229,366, Serial No. 09/573,081			PIF 00212 – 00316	Balakrishnan	
8	File History for U.S. Patent 4,811,075, Serial No. 07/041,994			PIF 00001 – 00076	Eklund	

* Exhibits from Fairchild's own files are admissions and therefore may not reference a particular sponsoring witness.

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
9	U.S. Patent No. 4,712,169 (Albach) with certificate of correction	'876 Patent	12/1987	PIF 08059 - 08066	Blauschild	
10	U.S. Patent No 4,930,063 (Henze *et al.*)	'876 Patent	05/1990	PIF 08229 - 08239	Blauschild	
11	U.S. Patent No. 5,459,392 (Mandelcorn)	'876 Patent	10/1995	PIF 08435 - 08443	Blauschild	
12	Ashok, Bindra, "Power-Conversion Chip Cuts Energy Wastage in Off-line Switchers"	'876 Patent	10/1998	PIF 08735 - 08739	Blauschild	
13	U.S. Patent No. 4,890,210 (Myers) with certificate of correction	'851/'366 Patents	12/1989	PIF 08205 - 08221	Blauschild	
14	U.S. Patent No. 5,014,178 (Balakrishnan)	'851/'366 Patents	05/1991	PIF 08294 - 08298	Blauschild	
15	U.S. Patent No. 5,034,871 (Okamoto *et al.*)	'851/'366 Patents	07/1991	PIF 08304 – 08315	Blauschild	
16	US Patent No. 5,041,956 (Marinus) with certificate of correction	'851/'366 Patents	08/1991	PIF 08316 – 08327	Blauschild	
17	Euro Pat. 0 748 034 A1 – H02M 3/00	'851/'366 Patents	12/1996	PIF 08664 – 08672	Blauschild	
18	Euro Pat. 0 748 035 A1 – H02M 3/155	'851/'366 Patents	12/1996	PIF 08673 – 08681	Blauschild	
19	B. Pelly et al, Power MOSFETs take the load off switching supply design, Electronic Design, Feb. 1983, pp 135-139.	'851/'366 Patents	02/1983	PIF 08765 – 08770	Blauschild	
20	U.S. Patent No. 5,245,526 Balakrishnan et al.	'366 Patent	09/1993	PIF 08377 – 08387	Blauschild	
21	U.S. Patent No. 4,626,879 Colak	'075 Patent	12/1986	PIF 08016 – 08022	Shields	
22	U.S. Patent No. 4,628,341 Thomas	'075 Patent	12/1986	PIF 08023 – 08032	Shields	
23	Sze, *Physics of Semiconductor Devices*, Wiley & Sons N.Y. c. 1981 pp. 431-438, 486-491	'075 Patent	1981	PIF 08716 – 08731	Shields	
24	http:/www.websters-online-dictionary.com/ definition/monolithic				Blauschild	N
25	FSD200, FSD201 Preliminary Specification, Fairchild Power Switch			FCS0625278 – 293	Blauschild	D, R, P, I
26	FSDL0365RNB, FSDM0365RNB Green Mode FPS datasheet			FCS0321469 – 488	Blauschild	
27	TNY256 (TinySwitch Plus) datasheet		08/1999	PIF31447 – 466	Balakrishnan, Blauschild	
28	TNY256 (TinySwitch Plus) datasheet		07/2001		Balakrishnan, Blauschild	N
29						
30						
31						
32	TNY256 schematic diagrams			PIF78050 – 061	Balakrishnan, Blauschild	R, P
33	TOP232 (TOP-FX) schematics			PIF19959 – 20110	Balakrishnan, Blauschild	R, P, I

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS	OBJECTION(S)
34	TOP232 (TOP-FX) datasheet		07/2001	PIF37480 – 515	Balakrishnan, Blauschild	
35	TOP242 (TOP-GX) datasheet		07/2001	PIF37516 – 563	Balakrishnan, Blauschild	
36	TOP249 (TOP-GX) schematics			PIF77019 – 037	Balakrishnan, Blauschild	
37	Klas Eklund Notes and documents	Eklund Ex. 5		KE00001 – 006	Eklund	R, P, H, F, A, I
38	Klas Eklund Notes and documents			KE00007 – 023	Eklund	R, P, H, F, A, I, T
39	Klas Eklund Notes and documents	Eklund Ex. 16		KE 00024 – 256	Eklund	R, P, H, F, A, I
40	Klas Eklund Notes and documents	Eklund Ex. 17		KE 00257 – 483	Eklund	R, P, H, F, A, I, T
41	Klas Eklund Notes and documents	Eklund Ex. 18		KE 00484 – 517	Eklund	R, P, H, F, A, I
42	Klas Eklund Notes and documents	Eklund Ex. 20		KE 00262 – 289	Eklund	R, P, H, F, A, I, T
43	Klas Eklund Notes and documents	Eklund Ex. 21		KE 00329 – 342	Eklund	R, P, H, F, A, I
44	Klas Eklund Notes and documents	Eklund Ex. 22		KE 00518 – 683	Eklund	R, P, H, F, A, I, T
45	Klas Eklund Notes and documents	Eklund Ex. 23		KE 00684 – 835	Eklund	R, P, H, F, A, I
46	Klas Eklund Notes and documents	Eklund Ex. 24		KE 00836 – 915	Eklund	R, P, H, F, A, I, T
47	Klas Eklund Notes and documents	Eklund Ex. 25		KE 00916 – 1090	Eklund	R, P, H, F, A, I
48	Klas Eklund Notes and documents	Eklund Ex. 26		KE 01091 – 1416	Eklund	R, P, H, F, A, I, T
49	Klas Eklund Notes and documents	Eklund Ex. 27		KE 01417 – 36	Eklund	R, P, H, F, A, I
50	Letter from Thomas Schatzel to Alys Hay re Klas Eklund	Eklund Ex. 8	04/07/88	KE 00012 – 14	Eklund	R, P, H, F, A, I, T
51	Letter from James Plummer to Bill Davidow re visit with Klaus Eklund, Art Fury and Alan Greben of Smartpower Inc.	Eklund Ex. 14	01/13/88		Eklund	R, P, H, F, A
52	Letter from Thomas Schatzel to George Honsbeen, II re Klas Eklund – Power Integrations	Eklund Ex. 15	07/17/91		Eklund	
53	Deutsche Bank Report, *Power Integrations: All charged up*		01/05/05	FCS0520731 – 68	Troxel	R, P, H, F, A
54	Piper Jaffray Co., *Note, Power Integrations, Inc.*		10/20/05	PIF92990 – 96	Renouard, Troxel	N
55	Citigroup Small/Mid-Cap Research, *Power Integrations Incorporated*		10/19/05	PIF93039 – 48	Renouard, Troxel	N

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
56	Technology License Agreement		06/29/00	PIF 23640 – 64	Balakrishnan, Renouard, Troxel	
57	Licensing and Wafer Supply Agreement		06/17/93	PIF 22638 – 67	Balakrishnan, Renouard, Troxel	N
58	MagneTek/Power Integrations Development and License Agreement		02/19/93	PIF 23511 – 46	Balakrishnan, Renouard, Troxel	
59	MagneTek Termination Agreement		12/22/04	PIF 23502 – 06	Balakrishnan, Renouard, Troxel	
60	MagneTek License Agreement		12/22/04	PIF 23494 – 501	Balakrishnan, Renouard, Troxel	
61	Patent License Agreement between American Telephone and Telegraph Company and Power Integrations, Inc.		06/11/92	PIF 23709 – 17	Balakrishnan, Renouard, Troxel	
62	*Power Integrations Fact Sheet*, Available from http://www.powerint.com/ir/docs/POWI_Fact_Sheet.pdf, downloaded 11/21/05		10/2005		Balakrishnan, Renouard, Troxel	N
63	Power Integrations, Inc. Annual Report Form for 10-K for the fiscal year ended December 31, 2002				Balakrishnan, Renouard, Troxel	N
64	Power Integrations, Inc. Annual Report Form 10-K for the fiscal year ended December 31, 2004			PIF61552 – 634	Balakrishnan, Renouard, Troxel	N
65	Fairchild Semiconductor International, Inc. Annual Report 10-K for the fiscal year ended December 31, 2001					N
66	Fairchild Semiconductor International, Inc. Annual Report 10-K for the fiscal year ended December 26, 2004			FCS1688403 – 575	Beaver	R, P, V
67	Email re Business Case and Questionnaire		12/17/03	FCS0673656 – 671	Troxel	I, R, P
68	Comparison Table – Middle Power			FCS0340728 – 730	Troxel	I, R, P
69	PDD Analog Green FPS			FCS0468433 – 449	Troxel	I, R, P
70	Charger Application, FPS Solution for Charger/Adaptor			FCS0513771 – 789	Troxel	I, R, P, H, F
71	Fairchild Power Switch, Power Conversion		09/2004	FCS0389879 – 390214	Troxel	H, F, R, P, V
72						
73	Development Plan for GFPS Product		01/2005	FCS0468450 – 470	Troxel	I, R, P

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
74	Field Test With FSD210 presentation by Jin-ho Choi			FCS0273256 – 267	Troxel	R, P, V, F, H
75	Fairchild & Samsung VD presentation		11/2004	FCS0543687 – 823	Troxel	R, P
76	FSCM0565R/FSCM0765R for STB, DVDR and LCD Monitor, Power Conversion Team, Power Supply Group		11/2004	FCS0290593 – 600	Troxel	R, P
77	Competition Review, v1.70		12/02/04	PIF39342 – 440	Renouard, Troxel	R, P, F, H, A
78	Amended and restated Wafer Supply Agreement b/t PI and Oki Electric Industry		04/01/03	PIF22744 – 771	Balakrishnan, Renouard, Troxel	
79	Wafer Supply Agreement b/t PI and ZMD Analog Mixed Signal Services		05/23/03	PIF22023 – 047	Balakrishnan, Renouard, Troxel	
80	Fairchild competition status report	Renouard Ex. 19	10/25/05	PIF88460 – 502 (electronic copy from CD37)	Renouard, Troxel	V, R, P, F, H, A, O
81	Fairchild Sales by Part and by Customer		2004-2005	FCS1231762 – 1811	Troxel	V, R, P, H, F
82	Fairchild Sales by Part and by Customer		2004-2005	FCS1686873 – 6925	Troxel	V, R, P, H, F
83	Weekly Sales Report		10/10/03	PIF 87080 – 87093	Renouard, Troxel	V, R, P, F, H, A, O
84	Weekly Sales Report		03/05/04	PIF 88093 –88104	Renouard, Troxel	V, R, P, F, H, A, O
85	Weekly Sales Report		10/22/04	PIF 87821 – 87836	Renouard, Troxel	V, R, P, F, H, A, O
86	Weekly Sales Report		2002	PIF 86660 – 86668	Renouard, Troxel	V, R, P, F, H, A, O
87	Weekly Sales Report		2002	PIF 86679 – 86688	Renouard, Troxel	V, R, P, F, H, A, O
88	Weekly Sales Report		07/03/02	PIF 86920 – 86929	Renouard, Troxel	V, R, P, F, H, A, O
89	Weekly Sales Report		08/08/03	PIF 87746 – 87764	Renouard, Troxel	V, R, P, F, H, A, O
90	Weekly Sales Report		10/03/03	PIF 87129 – 87143	Renouard, Troxel	V, R, P, F, H, A, O
91	Weekly Sales Report		10/31/03	PIF 87111 – 87128	Renouard, Troxel	V, R, P, F, H, A, O
92	Weekly Sales Report		02/20/04	PIF 88046 – 88058	Renouard, Troxel	V, R, P, F, H, A, O

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
93	Weekly Sales Report		04/09/04	PIF 88143 – 88153	Renouard, Troxel	V, R, P, F, H, A, O
94	Weekly Sales Report		04/04/03	PIF 87451 – 87472	Renouard, Troxel	V, R, P, F, H, A, O
95	Weekly Sales Report		07/11/03	PIF 87622 – 87635	Renouard, Troxel	V, R, P, F, H, A, O
96	Weekly Sales Report		08/22/03	PIF 87716 - 87732	Renouard, Troxel	V, R, P, F, H, A, O
97	Weekly Sales Report		08/29/03	PIF 87733 – 87745	Renouard, Troxel	V, R, P, F, H, A, O
98	Weekly Sales Report		02/06/04	PIF 88059 – 88070	Renouard, Troxel	V, R, P, F, H, A, O
99	Weekly Sales Report		08/09/02	PIF 86988 – 87001	Renouard, Troxel	V, R, P, F, H, A, O
100	Weekly Sales Report		01/17/03	PIF 87200 – 87215	Renouard, Troxel	V, R, P, F, H, A, O
101	Weekly Sales Report, "Korea, High, SEMCO"		12/03/04	PIF 87972 – 87976	Renouard, Troxel	V, R, P, F, H, A, O
102	CD containing Power Integrations electronic Point-of Sale Database (POS) data			PIF 095910 – 125226 (CD044)	Renouard, Troxel	R, P, Q
103	Quarterly Product Revenue and Standard Margin Analysis		04/11/02	PIF 54140 – 54192	Renouard, Troxel	R, P, H, F, A, V
104	Historical Revenue by Year, Product Family & Part #, 2004		2004	PIF 85559 – 85579	Renouard, Troxel	R, P, H, F, A, V
105	Historical Revenue by Year, Product Family & Part #, 2005		2005	PIF 85684 – 85705	Renouard, Troxel	R, P, H, F, A, V
106	Power Integrations revenue quantities by part number		2004-2005	PIF 144716 – 144737	Renouard, Troxel	R, P, H, F, A, V
107	Fairchild Tier 1 accounts list		2004-2005	FCS1686926 – 927	Troxel	R, P, V
108	FSDM0265RN Sales		2004	FCS1245900 – 903	Troxel	R, P, V
109	FSD210 Sales Bill and Booking	Jensen Ex. 4	2004	FCS1009945 – 957	Jensen, Troxel	D, R, P, F, H, A-C
110	Spreadsheet re sales by quarter with "Territory," "Product ID," and "Corp Cust"	Barnes Ex. 2	2004-2005	FCS 1688278 – 87	Barnes, Troxel	R, P, H, I, A, F
111	Spreadsheet re sales by quarter with "Territory," "Product ID," and "Corp Cust"	Barnes Ex. 3	2004-2005	FCS 1688288 – 94	Barnes, Troxel	R, P, H, A, F

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
112	Spreadsheet, "Historical Billing Data"	Barnes Ex. 4	2004-2005	FCS 1688295 – 319	Barnes, Troxel	R, P, H, A, F
113	Spreadsheet, "Green FPS 05 Proforma P&L"	Barnes Ex. 5	2005	FCS 1688322	Barnes, Troxel	
114	Spreadsheet, "Revenue & SM% FCST vs. ACT	Barnes Ex. 6	2004-2005	FCS 1688323	Barnes, Troxel	R, P, H, A, F
115	Spreadsheet	Barnes Ex. 7		FCS 1688324	Barnes, Troxel	R, P, H, A, F, I
116	Spreadsheet re sales	Barnes Ex. 8		FCS 1688325 – 26	Barnes, Troxel	R, P, H, A, F, I
117	Spreadsheet re end customers	Barnes Ex. 9	2004 – 05	FCS 1688327 – 65	Barnes, Troxel	R, P, H, A, F
118	Spreadsheet re sales	Barnes Ex. 10	2004 – 05	FCS 1688366 – 88	Barnes, Troxel	R, P, H, A, F
119	*High Voltage Dielectric Isolation SCR Integrated Circuit Process*, J.D. Beasom	Beasom Ex. 13			Beasom	
120	*Properties of dielectrially isolated integrated circuits*, J.D. Beasom and R.W. Randlett, Electronic Engineering	Beasom Ex. 14	11/1979		Beasom	
121	*A High Performance High Voltage Lateral PNP Structure*, James D. Beasom, IEEE	Beasom Ex. 15	1983		Beasom	
122	*A 500V Dielectric Isolation Process for Very High Voltage Integrated Circuits*, R.S. Pospisil, S.R. Jost, J.D. Beasom, Electro/86 and Mini/Micro Northeast-86 Conference Record	Beasom Ex. 16	05/13/86		Beasom	
123	*A 200V DI Process Which Provides IGT's, SCR's High Speed Complimentary Low Voltage Bipolars, CMOS and Bipolar Logic Options*, J.D. Beasom	Beasom Ex. 17	1987		Beasom	
124	WW Sales and Marketing	Beaver Ex. 1		FCS1688035 – 47	Beaver	R, P, H, A, F
125	The Power Franchise™ Marketing Update	Beaver Ex. 2	10/2005	FCS1687782 – 808	Beaver	R, P, H, A, F
126	E-mail from Sulekha Dhanota re price contract	Beaver Ex. 3	02/15/05	FCS1004572 – 74	Beaver	R, P, H, A-T, F, T, I
127	E-mail from Kirk Pond with Press Release	Beaver Ex. 4	02/17/04	FCS0516948 – 51	Beaver	R, P, H, A, F
128	E-mail from Robert Marston to George Farrales and Dan Godbout	Beaver Ex. 5	03/01/05	FCS1684981 – 84	Beaver	R, P, H, A, F
129	E-mail from Atman Chau to Terry Leung re Material for Tom Beaver	Beaver Ex. 6	11/10/04	FCS0667674 – 84	Beaver	R, P, H, A, F
130					Beaver	
131	E-mail from Alex Kwon re Weekly Report for Samsung account	Beaver Ex. 8	05/22/05	FCS1657110 – 11	Beaver	R, P, H, A, F
132	Agenda, Fairchild Korea Semiconductor, Ltd.	Beaver Ex. 9	04/12/04	FCS0467324 – 37	Beaver	R, P, H, A, F
133	E-mail from Youngsung Joo attaching LG RFQ	Beaver Ex. 10	12/01/04	FCS0657891 – 92	Beaver	R, P, H, A, F, T
134	E-mail from HK Kim re Road show for LG Group	Beaver Ex. 11	02/06/05	FCS0515661 – 62	Beaver	R, P, H, A, F
135						
136	Intel Presentation, Tom Beaver	Beaver Ex. 13	08/2004	FCS1680526 – 57	Beaver	R, P, H, A, F
137	DeWalt and Black & Decker Presentation	Beaver Ex. 14		FCS1459143 – 81	Beaver	R, P, H, A, F

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
138	Letters from Tom Beaver to customers	Beaver Ex. 15	12/23/04	FCS1688389 – 402	Beaver	R, P, I, H
139	E-mail from Corporate Communications	Beaver Ex. 16	10/25/04	FCS0336814 – 15	Beaver	R, P, H, A, F
140	Korean Letter from Tom Beaver re Power Integrations	Beaver Ex. 18		PIF144742	Beaver	R, P, I, H, T, F, A-T
141	Analyst Day Presentation, Tom Beaver	Beaver Ex. 19		FCS1631362 – 401	Beaver	R, P, H, F, A
142	Letter from Tom Beaver to Tim Jackson at GE		03/14/04	FCS1683987	Beaver	R, P
143	Fairchild Product Info Sheet re FSD210, FSD200	H.S. Choi Ex. 1	06/25/04	FCS0558997 – 014	Choi	
144	Product Info Sheet for FSDH321, FSDL321	H.S. Choi Ex. 2	10/01/04	FCS0326006 – 326025	Choi	
145	E-mail from Jonathan Harper re Green FPS Task Force Minutes	H.S. Choi Ex. 3	11/13/03	FCS0313542 – 313543	Choi	R, P, H
146	Green FPS Biz Review	H.S. Choi Ex. 4	11/06/03	FCS1023669 – 700	Choi	R, P, H
147	Design Tools: Green FPS Task Force	H.S. Choi Ex. 5	01/2004	FCS1174554 – 65	Choi	R, P, H
148	E-mail from HK Kim to Rexin Wang	H.S. Choi Ex. 6	02/06/04	FCS1113480 – 81	Choi	R, P, H
149	FSD210 Demo Board by H.S. Choi	H.S. Choi Ex. 7	02/02/04	FCS0616095 – 105	Choi	R, P
150	FSD210 Demo Board 3.3W battery charger	H.S. Choi Ex. 8	08/17/04	FCS0298666 – 70	Choi	R, P
151	Engineering Evaluation Demo Board Report using FSD210	H.S. Choi Ex. 9	08/28/04	FCS0394490 – 394520	Choi	F, A (not Fairchild document), R, P
152	DV-9.7W-FSDH0265RN Info Sheet	H.S. Choi Ex. 10		FCS0546374 – 75	Choi	R, P
153	DV-16W-FSDL0365RN Info Sheet	H.S. Choi Ex. 11		FCS0589740 – 41	Choi	R, P
154	E-mail from Brian Lavalle to Hang Seok Choi re Presentation material	H.S. Choi Ex. 12	10/21/03	FCS1117236 – 56	Choi	R, P
155	E-mail from Sang Tae Im to Brian Lavalle re Target FPS for STB	H.S. Choi Ex. 13	09/26/03	FCS0307788 – 307796	Choi	R, P
156	E-mail from Atman Chau to Choi et al. re RSDM05/0765R	H.S. Choi Ex. 14	03/15/04	FCS0312387 – 312412	Choi	R, P
157	E-mail from Seunghwan Lee to Sang Tae Im et al. re FPS with Frequency Modulation	H.S. Choi Ex. 15	12/08/03	FCS0676000 – 676035	Choi	R, P, H
158	E-mail from Hang Seok Choi to Chang re product development	H.S. Choi Ex. 16	08/03/03	FCS0692406	Choi	R, P, H, F
159	E-mail from Van Niemela to Hang Seok Choi et al. re FPS customer visits for Dr. Choi	H.S. Choi Ex. 17	07/14/03	FCS0316343 – 316349	Choi	R, P
160	Analog Application Engineering Group Weekly Report	H.S. Choi Ex. 18	08/14/03	FCS0643256 – 643274	Choi	R, P, T, F, A-T
161	E-mail from Seunghwan Lee to Hang Seok Choi et al. re SPI	H.S. Choi Ex. 19	11/23/03	FCS0654269	Choi	T, F, A-T, R, P, H

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
162	E-mail from HK Kim to Sang Tae Im re Samsung LCD Monitor	H.S. Choi Ex. 20	10/27/04	FCS0648715 – 648716	Choi	T, F, A-T, R, P, H, F
163	E-mail from Paul Kendle to Kevin Ream et al. re FPS with FM	H.S. Choi Ex. 21	12/05/03	FCS0698339 – 698341	Choi	R, P, H, F
164	E-mail from Hang Seok Choi to Jinho Choi et al. re Motorola	H.S. Choi Ex. 22	12/08/03	FCS0315727 – 315728	Choi	T, F, A-T, R, P, H
165	Taiwan/South China Business Trip Report, Hang-Seok Choi	H.S. Choi Ex. 23	01/02/05	FCS0415811 – 415815	Choi	R, P, H
166	Fairchild Power Switch PDD Analog	H.S. Choi Ex. 24	06/2003	FCS0396284 – 396481	Choi	R, P, H
167	Green FPS Fairchild Power Switch for Switch Mode Power Supplies	H.S. Choi Ex. 25	04/2004	FCS1038171 – 424	Choi	R, P, H
168	E-mail from Jintae Kim re WW50 weekly update for green FPS	Conrad Ex. 1	12/14/03	FCS1311754 – 55	Conrad	R, P
169	E-mail from Jong-Jib Kim to Bob Conrad re FPS Cost Analysis	Conrad Ex. 2	11/22/04	FCS0476719 – 476721	Conrad	R, P, H, F
170	E-mail from HK Kim to Bob Conrad, Hubertus Engelbrechten, and Dongyoung Huh re Green FPS support for design wins	Conrad Ex. 3	10/28/03	FCS1121139 – 1121141	Conrad	R, P
171	E-mail from HK Kim to Dongyoung Huh, Sangtae Im, Seunghwan Lee, and Sanghoon Jung re Green FPS support for design wins	Conrad Ex. 4	10/28/03	FCS1111927 – 1111929	Conrad	T, F, A-T, R, P
172	E-mail from Jong-Jib Kim to Minhwan Kim, Changki Jeon, and Cheoljoong Kim re the requirement for SDG5	Conrad Ex. 5	01/10/05	FCS1190656 – 1190659	Conrad	R, P, H, F
173	FSCM0565RD MOSFET line-up	Conrad Ex. 6	09/17/04	FCS0039327 – 39344	Conrad	R, P, H, F
174	ICG AOP R&D Overview, Bob Conrad	Conrad Ex. 7	2003-2004	FCS0491013 – 491034	Conrad	R, P
175	E-mail from Changsik Lim to Bob Conrad re SDG5	Conrad Ex. 8	01/09/05	FCS0519459 – 519490	Conrad	R, P, F
176	E-mail from Kyongmin Kim re WW47 weekly update for green FPS	Conrad Ex. 9	12/02/03	FCS0717502 – 717505	Conrad	T, F, A-T, R, P
177	Letters from Chris Bristow re IP issues	Conrad Ex. 26	01/12/06 01/13/06	FCS1689450 – 51	Conrad	
178	Letter from Tom Beaver to J.S. Min at Dongyang Instrument	Conrad Ex. 27	11/16/04	FCS1688393	Conrad	R, P
179	Motorola Business Review Presentation	Engelbrechten Ex. 2; Beaver Ex. 12	12/14/04	FCS1661968 – 2027	Engelbrechten, Beaver	R, P, H, F
180	ICG Communication Meeting Presentation Integrated Circuits Group, H. Engelbrechten	Engelbrechten Ex. 3	01/13/04	FCS1231702 – 1231733	Engelbrechten	R, P, H, F
181	E-mail from Terry Leung to Robert Gendron, et al. re New Transfer Business in 2005	Engelbrechten Ex. 4	01/17/05	FCS1660440 – 1660441	Engelbrechten	R, P, F

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
182						
183	E-mail from Sangtae Im to Oscar Freitas and Hangseok Choi re FPS promotion need for Q1'04	Gendron Ex. 2	11/11/03	FCS0311848 – 311851	Gendron	R, P, F
184	E-mail from Atman Chau to Ellen Lai, et al. re FSDM0265 & FSDL01665 price	Gendron Ex. 3	02/03/05	FCS0686479 – 686482	Gendron	R, P, F
185	E-mail from Kevin Ream to Robert Gendron, et al. re Americas Technical Sales and Marketing Weekly Report – WW50	Gendron Ex. 4	12/17/03	FCS1308850 – 1308852	Gendron	R, P
186	Spreadsheet re "Americas" sales for 2004 /2005	Godbout Ex. 1	2004-2005		Godbout	R, P, I
187	Fairchild Americas Presentation, Brent Rowe, RVP Americas	Godbout Ex. 2	04/2005	FCS1681117 – 58	Godbout	R, P, H, F
188	E-mail from Dan Godbout to Susan Douglass re Fairchild switcher formal quote – Sanyo/GE	Godbout Ex. 3	06/04/04	FCS1684670 – 1684674	Godbout	R, P, H, F
189	E-mail from Dan Godbout to Brent Rowe re GE/Fairchild switcher	Godbout Ex. 4	05/17/04	FCS1685251 – 55	Godbout	R, P, H, F
190	E-mail from Dan Godbout to Brent Rowe re GE formal quote	Godbout Ex. 5	05/18/04	FCS1683234 – 40	Godbout	R, P, H, F
191	E-mail from Dan Godbout to Brent Rowe, et al. re GE/Fairchild	Godbout Ex. 6	05/19/04	FCS1683941 – 47	Godbout	R, P, H, F
192	E-mail from Floyd Otto to Tim Sullivan, Dan Godbout, and Paul Kendle re Fairchild switcher control	Godbout Ex. 7	07/26/04	FCS1682045 – 48	Godbout	R, P, H, F
193	E-mail from Susan Douglass to Stephen West, et al. re PI Lawsuit	Godbout Ex. 8	04/04/05	FCS1684338 – 40	Godbout	R, P
194	Work-In-Progress, Resource Allocation by Project	J.S. Han Ex. 1	2003-2004	FCS1324258 – 59	Han	R, P
195	Work-In-Progress, Resource Allocation by Person	J.S. Han Ex. 2	2003-2004	FCS1324254 – 55	Han	R, P
196	Diagrams	J.S. Han Ex. 3	11/21/00	FCS0076787 – 76815	Han	
197	FSCM0565R Green Mode Fairchild Power Switch Info Sheet	J.S. Han Ex. 4	01/13/05		Han	
198	Diagrams (AR3656X-56)	J.S. Han Ex. 5		FCS0077356 – 80	Han	
199	FSCM0765R Green Mode Fairchild Power Switch Info Sheet	J.S. Han Ex. 6	02/14/05	FCS0628218 – 37	Han	
200	Fairchild Technical Report re AR3656X-76XX	J.S. Han Ex. 7	04/27/04	FCS0631171 – 91	Han	
201	Fairchild Technical Report re SDG4	J.S. Han Ex. 8	10/20/04	FCS0020878 – 98	Han	
202	Diagram by Designer Jinsub Han	J.S. Han Ex. 9	11/28/01	FCS0077050 – 70	Han	
203	Organizational Chart, Power Conversion, HK Kim,	S.T. Im Ex. 1	05/2005	FCS0524280	Im	
204	Korean Sales & Marketing Organization	S.T. Im Ex. 2	03/2005	FCS0524276 – 77	Im	
205	Product Strategy Fairchild Power Switch	S.T. Im Ex. 3	08/2001	FCS1097612 – 29	Im	R, P, H, F
206	Strategic Business Plan, Power Conversion, HK Kim	S.T. Im Ex. 4	10/2003	FCS0613756 – 89	Im	R, P, H, F
207	Power Supply Strategy, Power Conversion	S.T. Im Ex. 5	07/28/04	FCS0640957 – 1009	Im	R, P, H, F

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
208	Project/Customer Spreadsheet	S.T. Im Ex. 6		FCS0683113 – 22	Im	R, P
209	Green FPS (Power Saver) Launching Plan	S.T. Im Ex. 7	08/29/03	FCS0641675 – 93	Im	R, P, H, F
210	PD Analog Business Review	S.T. Im Ex. 8	03/10/03	FCS0507189 – 223	Im	R, P, H, F
211	Power Conversion Biz Review	S.T. Im Ex. 9	01/12/04	FCS0608236 – 87	Im	R, P, H, F
212	Product Strategies for SPS & STD ICs	S.T. Im Ex. 10	05/09/00	FCS0503931 – 80	Im	R, P, H, F
213	Power Conversion Regional Marketing Meeting at Bucheon Korea	S.T. Im Ex. 11	04/21/04	FCS0681900 – 2017	Im, Troxel	R, P, H, F
214	AP FPS Plan	S.T. Im Ex. 12	12/15/02	FCS0682646 – 68	Im	R, P, F, H, V
215	Fairchild presentation entitled PDD Analog *Marketing*, FY03 Q2 QBR	S.T. Im Ex. 13	07/2003	FCS0610280 – 337	Im	R, P
216	PDD Analog Strategic Direction for Q4 2003	S.T. Im Ex. 14	09/2003	FCS0674491 – 505	Im	R, P, H, F
217	Power Conversion Biz Review, HK Kim	S.T. Im Ex. 15	07/2004	FCS0083906 – 819	Im	R, P
218	Spreadsheet re Opportunity for PDD Analog over WW	S.T. Im Ex. 16	01/09/04	FCS0705368 – 83	Im	R, P
219	Power Conversion Weekly Report WW05	S.T. Im Ex. 17		FCS1015860 – 89	Im	R, P
220	Spreadsheet re Bill & BKG_CY04	S.T. Im Ex. 18	08/05/04	FCS0558111 – 28	Im	R, P
221	Green FPS Fairchild Power Switch for Switch Mode Power Supplies	S.T. Im Ex. 19	04/2004	FCS1104208 – 53	Im	R, P, H, F
222	E-mail from Seunghwan Lee to Taehyun Kim re Green FPS	S.T. Im Ex. 20	08/11/03	FCS0669132 – 40	Im	R, P, T, F, A-T, H
223	E-mail from Seunghwan Lee to HK Kim re TOP 12 Program	S.T. Im Ex. 21	03/04/04	FCS1118480 – 97	Im	R, P, T, F, A-T
224	E-mail from Sangtae Im to Atman Chau re SPI for Samsung	S.T. Im Ex. 22	11/28/04	FCS0660739 – 42	Im	R, P, F, H
225	E-mail from Alan Hu to Atman Chau re SPI/Supreme	S.T. Im Ex. 23	12/26/04	FCS0659728 – 30	Im	R, P, F, H
226	E-mail from Robin Zhang to Sangtae Im re 10watt charger	S.T. Im Ex. 24	11/10/04	FCS0339576	Im	R, P
227	E-mail from Chuil Park to Danny Lin re PL for PC	S.T. Im Ex. 25	05/10/04	FCS0676533 – 40	Im	R, P, H, F
228	E-mail from Seunghwan Lee to Atman Chau re Green FPS	S.T. Im Ex. 26	08/14/03	FCS0648686 – 87	Im	R, P
229	E-mail from HK Kim to Changsik Lim re Hughes FSCM0765RD	S.T. Im Ex. 27	08/29/03	FCS0520709 – 12	Im	R, P
230	E-mail from Brent Markman to Sangtae Im et al. re Xbox	S.T. Im Ex. 28	05/12/03	FCS0309575	Im	R, P, H, F
231	Fairchild Semiconductor FSDH0165	K.O. Jang Ex. 1	09/21/00	FCS0146190 – 99	Jang	
232	Technical Report	K.O. Jang Ex. 2	03/24/99	FCS0354603 – 43	Jang	
233	Fairchild Semiconductor FSD200 Fairchild Power Switch (FPS)	K.O. Jang Ex. 3	11/20/03	FCS0562318 – 29	Jang	
234	Fairchild Semiconductor FSD200, FSD201 Fairchild Power Switch	K.O. Jang Ex. 4	07/09/03	FCS0619789 – 9800	Jang, Blauschild	R, P
235	Fairchild Semiconductor FSD210H Green Mode 700 V	K.O. Jang Ex. 5	10/07/04	FCS0597922 – 37	Jang	
236	Fairchild Semiconductor FSDM311 Fairchild Power Switch (FPS)	K.O. Jang Ex. 6	11/11/03	FCS0553036 – 45	Jang	
237	Fairchild Semiconductor FSDL365RN, FSDM365RN datasheet	K.O. Jang Ex. 7	06/17/04	FCS0344990 – 5011	Jang	

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
238	Fairchild Semiconductor FSDL0365RNB, FSDM0365RNB datasheet	K.O. Jang Ex. 8	04/26/05		Jang	
239	Fairchild Semiconductor FSD210 Fairchild Power Switch (FPS)	K.O. Jang Ex. 9	02/26/03	FCS0471645 – 52	Jang	R, P
240	Fairchild Semiconductor FSD21x-Series FSD210, FSD211	K.O. Jang Ex. 10	07/09/03	FCS0617260 – 71	Jang	R, P
241	FSD210 schematics	K.O. Jang Ex. 11	07/18/03	FCS0026915 – 60	Jang	M
242	R&D Plan	K.O. Jang Ex. 12	09/17/03	FCS0128753 – 75	Jang	
243	The Power Franchise booklet	K.O. Jang Ex. 13		FCS0015443 – 70	Jang	
244	FSD211H Design Review2	K.O. Jang Ex. 14	01/19/05	FCS0123427 – 36	Jang	
245	FSDH321 schematics	K.O. Jang Ex. 15	12/12/03	FCS0077290 – 317	Jang	M, R, P, I, D
246	FSDL0365RNB schematics	K.O. Jang Ex. 16	12/12/03	FCS0077092 – 124	Jang	M
247	Technical Report	K.O. Jang Ex. 17	05/07/04	FCS0010192 – 229	Jang	
248	Product Development Tracking	K.O. Jang Ex. 18		FCS0129047 – 49	Jang	R, P, F, A, H
249	FSDM311 schematics	K.O. Jang Ex. 19	11/09/04	FCS0077017 – 40	Jang	M
250	Technical Report	K.O. Jang Ex. 20	07/07/04	FCS0002902 – 39	Jang	R, P
251	Fairchild Semiconductor FSDM0265RNC	K.O. Jang Ex. 21	02/26/04	FCS0546429 – 46	Jang	R, P
252	Fairchild PWM Control IC (FAN7602)	K.O. Jang Ex. 22	10/2003	FCS0618772 – 86	Jang	R, P
253	Frequency Modulation for the EMI (Electromagnetic Interference)	K.O. Jang Ex. 23		FCS0142533 – 48	Jang	
254	Frequency Modulation for the EMI (Electromagnetic Interference)	K.O. Jang Ex. 24		FCS0099595 – 610	Jang	
255	The 24th Weekly Report of SPS Group 2001 6. 16.	K.O. Jang Ex. 25	06/16/01	FCS0486685 – 89	Jang	R, P
256	Extending Power Capability While Simplifying Design Process	K.O. Jang Ex. 26	03/2001	FCS1173125 – 27	Jang	R, P, H
257	E-mail re Frequency Jitter with US Patent attached, Patent number 6,229,366	K.O. Jang Ex. 28	06/13/01	FCS0704049 – 67	Jang	T, I, F, A-T, R, P
258	Oscillator and DAC in FPS	K.O. Jang Ex. 30		WOO 00001 – 00005	Jang	R, P, F, A
259	Business Object Report	Jensen Ex. 2	2004-2005	FCS1685950 – 54	Jensen	R, P, I
260	Opportunity for PDD Analog Over WW	Jensen Ex. 3	02/26/04	FCS0611037 – 84	Jensen	R, P, F, A-C, H
261	FSCQ-Series Sales to Samsung; FAN7601 Sales: 2003-2004; etc.	Jensen Ex. 4	06/01/04		Jensen	D, R, P, F, A-C, H
262	Product Sales: 2004-2005	Jensen Ex. 5	2004-2005		Jensen	R, P, F, A-C, H
263	Sales of Products from 2001Q1-2004Q3	Jensen Ex. 6	2001-2004		Jensen	R, P, F, A-C, H
264	Rep Presidents Meeting (Welcome to South Portland)	Jensen Ex. 7	10/21/03	FCS1473050 – 150	Jensen	R, P, F, H
265	Geography Segment	Jensen Ex. 8	08/19/04	FCS1613137 – 69	Jensen	R, P, H, F

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
266	Fairchild Semiconductor presentation (title obscured by ink)	Jensen Ex. 9		FCS1444973 – 5006	Jensen	R, P, H, F
267	E-mail from Stephen Jensen to Robert Gendron re Control4 Merlin	Jensen Ex. 10	02/24/05	FCS1555699 – 700	Jensen	R, P, H, F
268	Quarterly Business Review – Americas Business Marketing	Jensen Ex. 11	02/2003	FCS1084979 – 5042	Jensen	R, P
269	Geographies Segment Regional Sales Update	Jensen Ex. 12	02/2003	FCS1099279 – 341	Jensen	R, P
270	Fairchild Semiconductor presentation (title obscured by ink)	Jensen Ex. 13		FCS1435108 – 32	Jensen	R, P, H, F
271	Fairchild Semiconductor presentation (title obscured by ink)	Jensen Ex. 14		FCS1469915 – 63	Jensen	R, P, H, F
272	650V/1A, SPS 1-chip Process	C.K. Jeon Ex. 2		FCS0176604 – 24	Jeon	
273	R&D Specification, SDG3(TE1 403X) Design Manual	C.K. Jeon Ex. 3	02/20/02	FCS0173478 – 506	Jeon	
274	The Research of HV-BCDMOS(SDG3) Process	C.K. Jeon Ex. 4	02/17/02	FCS0194520 – 35	Jeon	
275	700V BCDMOS Process with 1.2μm Design Rule	C.K. Jeon Ex. 5	05/19/00	FCS0189639 –60	Jeon	
276	R&D Specification, SDG4(TE1 407X) Design Manual	C.K. Jeon Ex. 6	07/01/01	FCS0186368 – 409	Jeon	
277	R&D Specification, SDG4(TE1 421X) Design Manual	C.K. Jeon Ex. 7	07/22/02	FCS0019645 – 87	Jeon	
278	R&D Specification, SDG4(TE1 421X) Design Manual	C.K. Jeon Ex. 8	07/02/03	FCS0209265 – 325	Jeon	
279	Technical Report, SDG4(TE1 421X 1.2um 700V)	C.K. Jeon Ex. 9	07/23/02	FCS0247915 – 46	Jeon	
280	R&D Specification TE1407X-01XX	C.K. Jeon Ex. 10	06/10/02	FCS1685695 – 721	Jeon	
281	R&D Specification, SDG4(TEA 421X) Design Manuel	C.K. Jeon Ex. 11	11/24/03	FCS1685618 – 52	Jeon	
282	Qualification Plan	C.K. Jeon Ex. 12	06/10/04	FCS0037736 – 54	Jeon	R, P
283	R&D Specification, SDG4 Process Standard Data Book	C.K. Jeon Ex. 13	02/11/01	FCS1685653 – 82	Jeon	
284	R&D Specification, SDG4 TE1421X Design Manual	C.K. Jeon Ex. 14	07/19/02	FCS0018803 – 42	Jeon	
285	R&D Specification, SDG4 Design Manual	C.K. Jeon Ex. 15	11/02/04	FCS1685560 – 617	Jeon	
286	R&D Specification, SDG3(TE1 403X) Design Manual	C.K. Jeon Ex. 16	10/23/00	FCS1332212 – 40	Jeon	
287	Introduction of SDG3/ SDG4 Process HV Part	C.K. Jeon Ex. 21	04/2003	FCS0468204 – 36	Jeon	
288	SDG4 NTPRS Phase 2	C.K. Jeon Ex. 22	07/23/02	FCS0037052 – 143	Jeon	R, P
289	650V	C.K. Jeon Ex. 23		FCS1329257 – 69	Jeon	T, I, F, A-T
290	Rugged MOSFET (LDMOS vs. VDMOS)?	C.K. Jeon Ex. 24		FCS0407439	Jeon	I, R, P
291	Process Development Group Weekly Report (CY02:11/08-11/14)	C.K. Jeon Ex. 25		FCS0455243 – 49	Jeon	R, P
292	Process Development Group Weekly Report (CY02:11/29-12/05)	C.K. Jeon Ex. 26		FCS0446617 – 23	Jeon	R, P
293	Technical Report, PI, TNY266P Construction Analysis	C.K. Jeon Ex. 27	12/11/02	FCS1685523 – 59	Jeon	R, P
294	E-mail from Jongjib Kim to Minhwan Kim re FPS Cost Analysis	C.K. Jeon Ex. 28	11/14/04	FCS0252710 – 16	Jeon	T, I, F, A-T, H, R, P
295	Development Plan for GFPS Product 2005.2 Process Development	C.K. Jeon Ex. 29	02/2005	FCS0459111 – 38	Jeon	R, P, H
296	Technical Report	C.K. Jeon Ex. 31	03/03/99	FCS1330824 – 33	Jeon	T, I, F, A-T,

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
297	The Power Franchise	C.K. Jeon Ex. 32		FCS1413738	Jeon	I
298	R&D Specification, SDG3 (TE1403X) Design Manual	C.K. Jeon Ex. 33	02/20/02		Jeon	
299	High Voltage MOS Transistors	C.K. Jeon Ex. 34			Jeon	M
300	BCD SPS Development Plan	C.S. Lim Ex. 1	07/15/02	FCS0494668 – 72	Lim	R, P, T, I, F, A-T
301	E-mail from HK Kim to Changsik Lim re: FPS 2004 development	C.S. Lim Ex. 2	08/21/03	FCS0518029 – 34	Lim	R, I, F, A, R, P
302	E-mail from Terry Johnson to Sangtae IM re: Green FPS update	C.S. Lim Ex. 3	07/08/03	FCS0514354 – 59	Lim	R, P
303	E-mail from Oscar Freitas to Terry Johnson re: San Jose trip report	C.S. Lim Ex. 4	08/15/03	FCS0520806 – 09	Lim	R, P, H, F
304	E-mail from Changsik Lim to Oscar Freitas re: AN-4137 edits	C.S. Lim Ex. 5	12/17/03	FCS1010471 – 74	Lim	R, P, H, F
305	E-mail from Bob Conrad to Changsik Lim re: requirement for SDG5	C.S. Lim Ex. 6	01/06/05	FCS0517284	Lim	R, P, H, F
306	E-mail from C.S. Lim to DeokJung Kim re: list of relevant patents	C.S. Lim Ex. 7	02/03/03	FCS1006486 – 87	Lim	R, P, T, I, F, A-T, M
307	Comparison & Analysis of Patent PI (US 6,249,876) vs. FSC (Frequency Modulation)	C.S. Lim Ex. 8		FCS0577195 – 198	Lim	BN
308	Americas and Europe Regional Update	Rowe Ex. 1	11/24/03	FCS1474179 – 1474296	Rowe	R, P, H, F
309	Enabling Emerson Success – Fairchild Semiconductor	Rowe Ex. 2	05/19/04	FCS1459364 – 1459437	Rowe	R, P, H, F
310	Letter from John Corbett to Brent Rowe re a co-written paper	Rowe Ex. 3	03/17/04	FCS1602060 – 62	Rowe	R, P
311	Spreadsheet re Projects	Rowe Ex. 4		FCS1681735 – 41	Rowe	R, P, H, F
312	Intel Quarterly Business Review	Rowe Ex. 5	09/01/04	FCS1674956 – 5038	Rowe	R, P, H, F
313	Key Product Activity Update	Rowe Ex. 6		FCS1678262 – 77	Rowe	R, P
314						
315						
316						
317						
318	S.G. Cowen Analyst Report	Slayton Ex. 2	02/03/06	FCS1690338 – 56	Slayton, Troxel	R, P, H, F, A, V
319	S.G. Cowen Analyst Report		12/08/05	FCS1690357 – 84	Keeley, Troxel	R, P, H, F, A, V
320	S.G. Cowen Analyst Report	Slayton Ex. 6	07/14/04	FCS1690161 – 208	Slayton, Troxel	R, P, H, F, A, V
321	Presentation regarding Fairchild Power Switch (FPS)	Beaver Ex. 7	06/2005	FCS1687871 – 98	Beaver	R, P, H, A, F, D
322	Fairchild list of products in the Off-Line Conversion IC – Power Switch product family			FCS1693068 – 73		
323	Fairchild list of products in the Green FPS product family			FCS1693074 – 76		

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
324	PI PowerPoint re Manufacturing Proposal for Solectron	Bailey Ex. 8		PIF94787-PIF94805	Balakrishnan, Renouard	
325	PI Invention Disclosure Form	Balakrishnan Ex. 17		PIF63306-PIF63313	Balakrishnan	
326	PI Invention Disclosure Form	Balakrishnan Ex. 16		PIF63314-PIF63324	Balakrishnan	
327	E-mail from Atman Chau re FSDM0265RN/Customer_Set Survey		10/21/04	FCS0662533 – 540		R, P, T, A-T, H, F, V
328	E-mail from Bruce Renouard to Richard Fassler attaching Sales Mtg Action Items 6-25-04 spreadsheet		06/25/04	PIEM0001246 – 1250	Renouard	R, P, V, H, F, A
329	E-mail from Bruce Renouard to Cliff Walker re Fairchild competition update		03/31/04	PIF 38114	Renouard	R, P, V, H, F, A
330	Fairchild Semiconductor Investor Fact Book from Fairchild's website		2005		Conrad, Beaver	N
331	Investor Relations, Corporate Profile, Geographic Footprint Overview http://investor.fairchildsemi.com/phoenix.zhtml?c=118532&p=irol-homeprofile		04/13/06 Print date		Conrad, Beaver	N
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333	Memo from Scott Garrard and CS Song to Don Desbiens re R&D Guidelines		07/24/01	FCS0445538 – 39		R, P
334	Design/Process Change Notification – Final	Kim Ex. 1		FCS1661316 – 1317	Kim	R, P, D
335	E-mail from HK Kim	Kim Ex. 2	02/04/05	FCS0415484 – 513	Kim	T, A-T
336	E-mail from Jonathan Harper	Kim Ex. 3	12/08/03	FCS0307103 – 108	Kim	R, P, H, F
337	Power Conversion Workshop booklet	Kim Ex. 4	07/16/04	FCS0502443 – 530	Kim	T, A-T, R, P, H, F
338	E-mail from HK Kim to Sangtae Im	Kim Ex. 5	10/27/04	FCS1111840 – 841	Kim	R, P, H, F
339	E-mail from Robert Gendron to Brent Rowe	Kim Ex. 6	07/14/03	FCS0307176 – 181	Kim	R, P, V
340	E-mail from Chau to Kang; HK Kim	Kim Ex. 7	11/04/03	FCS0645563 – 566	Kim	R, P, V
341	E-mail from Soonhong Park	Kim Ex. 8	01/23/05	FCS0517053 – 54	Kim	R, P, H, F
342	E-mail from Dan Godbout to Sangtae Im	Kim Ex. 9	08/21/03	FCS0307884 – 887	Kim	R, P, V
343	E-mail from HK Kim to Terry Johnson	Kim Ex. 10	10/28/03	FCS1119566 – 567	Kim	R, P, V
344	E-mail from HK Kim	Kim Ex. 11	02/10/05	FCS0652361 – 363	Kim	R, P
345	E-mail from Jintae Kim to Robert Gendron	Kim Ex. 12	02/06/05	FCS1666591	Kim	R, P, F, H, I
346	E-mail from Sangtae Im to Seunghwan Lee	Kim Ex. 13	08/17/03	FCS0651431 – 432	Kim	R, P, V

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
347	Top 210 reverse engineered schematics			FCS0541094 – 1120		R, P
348	TNY264 reverse engineered schematics			FCS0541121 – 31		BN
349	TNY264 reverse engineered schematics			FCS0539827 – 29		R, P
350	Fairchild sales data			FCS0668851 – 964		R, P, V
351	Fairchild Intel customer file			FCS1686162 – 80		M, R, P, V
352	Fairchild Intel customer file			FCS1686204 – 29		M, R, P, V
353	Fairchild Intelbras customer file			FCS1686230 – 47		M, R, P, V
354	Fairchild Microsoft customer file			FCS1686250 – 65		M, R, P, V
355	Fairchild Thomas & Betts customer file			FCS1686311 – 32		M, R, P, V
356	Fairchild Motorola FSDH0265 file			FCS1686551 – 54		M, R, P, V
357	Fairchild Phihong FSD210 file			FCS1686564 – 88		M, R, P, V
358	Fairchild Whirlpool FSDM0365 file			FCS1686602 – 28		M, R, P, V
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360	PI Excel sheet: "Identified Lost Business"	FCS Ex. 161		PIEM0005972 – 82	Renouard	
361	Power Integrations' Product Selector Guide, available online at http://www.powerint.com/PDFFiles/selectorguide.pdf	FCS Ex. 182	June 2006		Balakrishnan, Renouard	
362	NPD Group article – "U.S. Mobile Phone Sales Reached 31.6 Million Units in Third Quarter 2005"	Troxel Ex. 40; FCS Ex. 527	10/24/05		Troxel	
363	IDC – "Worldwide Mobile Phone Market Breaks 200 Million Unit Mark in 3Q05"	Troxel Ex. 41; FCS Ex. 528	10/20/05		Troxel	
364	DisplaySearch – "Report Indicates Q1 '05 LCD Desktop Monitors Rise 7% Q/Q"	Troxel Ex. 42; FCS Ex. 529	06/21/05		Troxel	
365	Fairchild Design Wins Spreadsheet	FCS Ex. 533		Excel spreadsheet; also produced at FCS1689437 – 39		
366	Fairchild Design Wins Spreadsheet	FCS Ex. 533		Excel spreadsheet; also produced at FCS1689440 – 49		
367	PI Excel sheet: "Identified Lost Business"	FCS Ex. 161		PIEM0005972 – 82	Renouard	
368	Press Release, "Power Integrations Awarded 'Product of the Year' in 'Green' Technology"		03/09/04	PIF 131300	Balakrishnan	F, H, R, P
369	Press Release, "Power Integrations Receives Product of the Year Award from Electronic Products Magazine"		01/22/03	PIF 131300	Balakrishnan	F, H, R, P
370	Press Release, "President Bush Issues Order to Slay Energy Vampires"		07/31/01	PIF 131300	Balakrishnan	F, H, R, P
371	Press Release, " Power Integrations to be Featured on 'Business Now' Television This Weekend"		07/11/01	PIF 131300	Balakrishnan	F, H, R, P

TRIAL EX. NO.	DESCRIPTION OF EXHIBIT	DESIGNATED AT/IN	DATE	BATES RANGE	SPONSORING WITNESS*	OBJECTION(S)
372	Press Release, "Power Integrations Gives 'Vampire' Demonstration to President George W. Bush"		06/28/01	PIF 131300	Balakrishnan	F, H, R, P
373	Press Release, "First Monolithic High-Voltage Power Conversion IC Family to Deliver Up to 250 Watts"		11/20/00	PIF 131300	Balakrishnan	F, H, R, P
374	Press Release, "Power Integrations Introduces the Highest Level of System Integration with TOPSwitch-FX® Power Conversion ICs"		03/20/00	PIF 131300	Balakrishnan	F, H, R, P
375	Press Release, "Power Integrations Selected as Finalist in 1999 Discover Awards for Technological Innovation"		04/29/99	PIF 131300	Balakrishnan	F, H, R, P
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378	"Electronics and IT Industry Leaders Meet to Share Technologies and Strategies for Improving Energy Efficiency in Power Supplies," Energy Star News Archive		01/2002	PIF 62655 – 62670	Balakrishnan	F, H, R, P
379	CD containing electronic copy of Fairchild shipment document regarding FSD210HD manufactured within the U.S.			FCS1691603 (CD)	Dupuis	R, P-NAD
380	Fairchild shipment document printout regarding FSD210HD manufactured within the U.S.	Dupuis Ex. 5	2004-2006	FCS1691604 – 717	Dupuis	R, P-NAD
381	SDG4 Process Transfer document	Dupuis Ex. 6	02/12/04	FCS1693108 – 17	Dupuis	
382	Fairchild wafer starts profile	Dupuis Ex. 7	2004-2005	FCS1693118	Dupuis	
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EXHIBITS 3 – 8

REDACTED IN THEIR ENTIRETY

EXHIBIT 9

United States Patent [19]

Beasom

[11] **Patent Number: 4,823,173**

[45] **Date of Patent: Apr. 18, 1989**

[54] **HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION**

[75] Inventor: **James D. Beasom**, Melbourne Village, Fla.

[73] Assignee: **Harris Corporation**, Melbourne, Fla.

[21] Appl. No.: **831,384**

[22] Filed: **Jan. 7, 1986**

[51] **Int. Cl.**[4] **H01L 29/80**

[52] **U.S. Cl.** **357/22**; 357/23.8; 357/35

[58] **Field of Search** ..... 357/23.8, 22 E, 22 F, 357/22 G, 35

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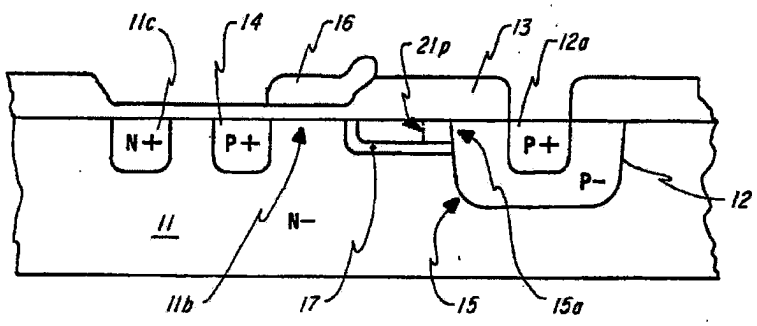
Primary Examiner—Joseph E. Clawson, Jr.
Attorney, Agent, or Firm—William A. Troner; Charles C. Krawczyk

[57] **ABSTRACT**

The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired. A top gate of the same conductivity type as the device region with which it is associated is provided along the surface of the substrate and overlying the lateral drift region. In an MOS device, the extremity of the lateral drift region curves up to the substrate surface beyond the extremity of the top gate to thereby provide contact between the JFET channel and the MOS channel.

19 Claims, 3 Drawing Sheets



Case No. 04-1371-JJF
DEFT Exhibit No. DX 541
Date Entered _____
Signature _____

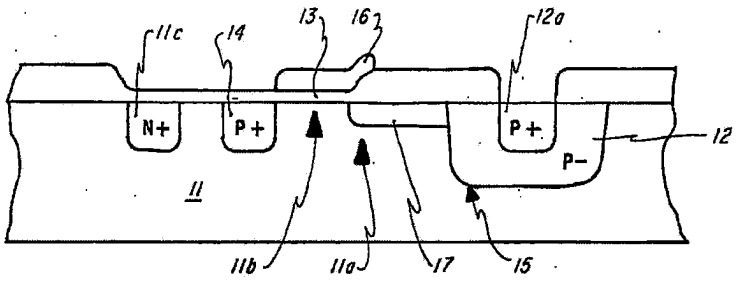


FIG. 1

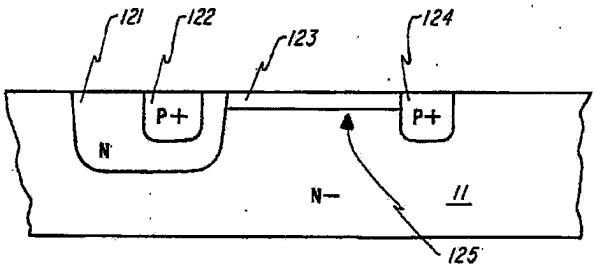


FIG. 2

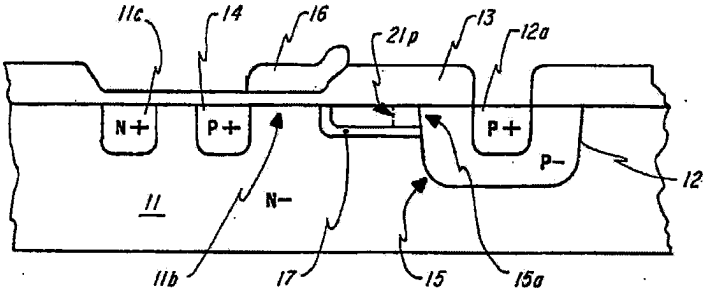


FIG. 3

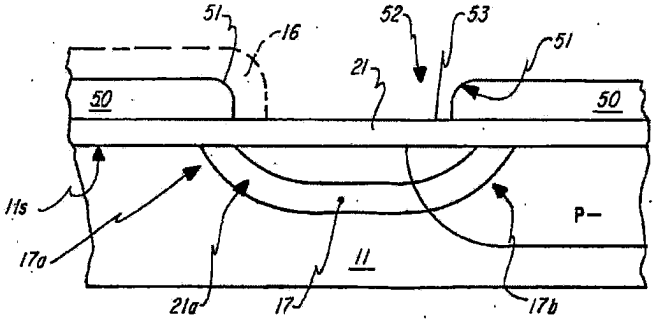


FIG. 4

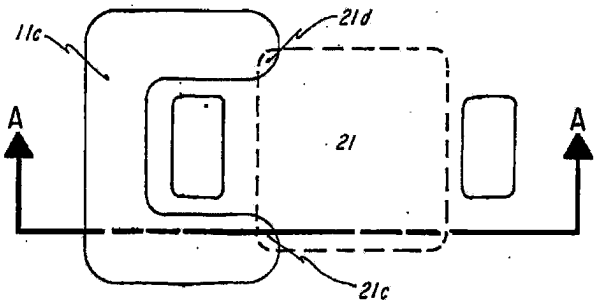


FIG. 5a

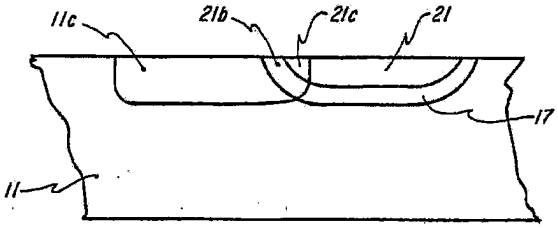


FIG. 5b

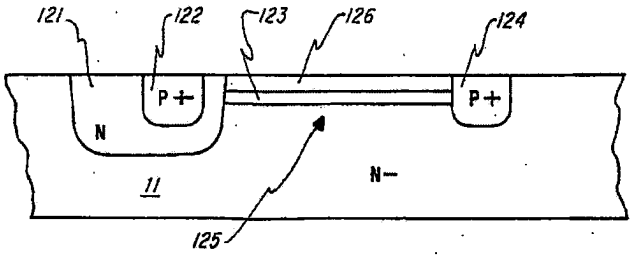


FIG. 6

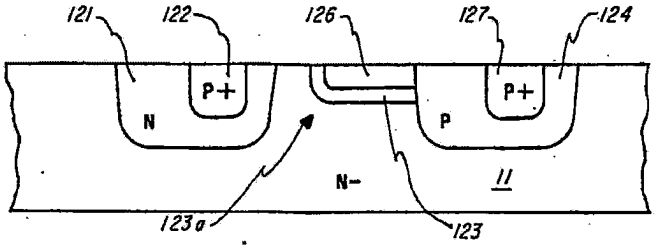


FIG. 7

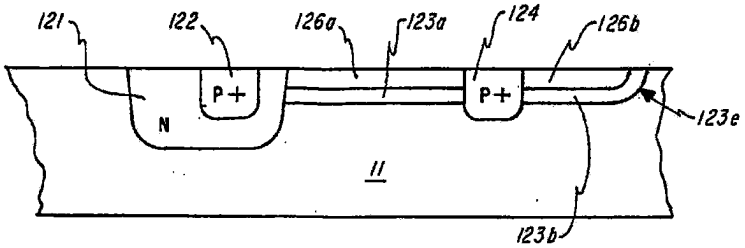


FIG. 8

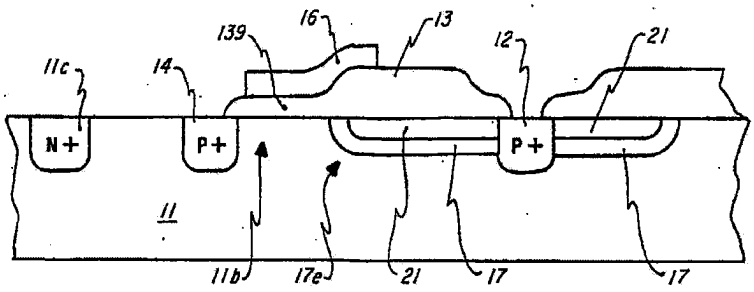


FIG. 9

HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION

FIELD OF THE INVENTION

The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices.

Previous high voltage lateral devices include both MOS devices and bipolar transistors. For example, FIG. 1 illustrates a known structure which can be used as a high voltage lateral MOS device. This device is known as a lateral drift region MOS device and is dependent upon the drain body junction **15** as the basic high voltage junction of the device. The drift region **17** is a P region along the top surface of the N^{31} substrate **11** and is located so as to lie adjacent the P− drain region **12**. The drift region **17** is used to connect the high voltage drain **12** to the gate **16** and source **14**. The two contacts, drain contact 12_a and body contact 11_c are shown for completeness. In the operation of this circuit, the gate **16** and source **14** never assume large voltages relative to the body **11**. The drift region **17** serves as a JFET channel with the portion 11_a of body region **11** underlying the channel acting as a JFET gate. The JFET channel **17** is designed to totally deplete when the drain **12** is reverse biased to a voltage less than the voltage necessary to reach critical field in the channel to body depletion layer. This design preserves the effective high breakdown voltage of drain body junction **15**. Also, the source **14** and gate **16** (over the gate oxide **13**) are safely shielded from the high drain body voltage by the pinched off JFET channel **17**.

The resistance of the lateral drift region JFET channel **17** is in series with the resistance of the MOS channel 11_b, consequently the total channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltages, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

FIG. 2 shows a known structure which can be used as a lateral bipolar transistor. Another illustration of such a device is contained in FIG. 7 of U.S. Pat. No. 4,283,236 issued Aug. 11, 1981. Referring to FIG. 2, an N− substrate **11**, has an N type emitter shield **121** formed therein and P+ emitter **122** and collector **124** located as shown. Additionally, a P− drift region **123** is provided along the surface of the substrate between the collector **124** and the emitter shield **121**. In this device, the total collector resistance is equal to the sum of the resistance across the drift region **125** plus the resistance of the P+ collector between the drift region and the collector contact. In order to provide devices of equal size having a lower collector resistance, it is desirable to find ways to reduce the resistance of the drift region.

In the operation of this device, the drift region extends the collector to the edge of the emitter shield, **121**, so that the base width is just that small distance between the adjacent edges of the emitter, **121**, and the drift region, therefore providing improved frequency response.

At high base collector voltages the drift region, **123**, depletes by JFET action with the N-base, **11**, and N

shield, **121**, which is part of the base, acting as gate before critical field is reached just as for the MOS of FIG. 1. This preserves the high breakdown of the structure.

SUMMARY OF THE INVENTION

The present invention provides a structure having a reduced channel resistance and a process capable of efficiently obtaining the structure of the invention. The reduction in channel resistance is accomplished by providing a top gate which is located between the lateral drift region of the prior art and the surface of the channel region and which may be in contact with the high voltage device region. This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. The ionized channel impurity atoms associated with this additional channel charge causes the reduction in channel resistance.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross section of a known MOS device having typical ON resistance.

FIG. **2** is a cross section of a known bipolar transistor having typical collector resistance.

FIG. **3** is a cross section of an MOS device including the improved drift region and top gate of the invention.

FIG. **4** illustrates optimized process steps for obtaining the desired shape of the top gate and drift region of the invention.

FIGS. *5a* and *5b* are respectively a top view and is a cutaway perspective view of the body contact extending through the top gate and drift region of the invention.

FIG. **6** is a cross section of a bipolar device made in accordance with one aspect of the invention.

FIG. **7** is a cross section of a bipolar device made in accordance with another aspect of the invention.

FIG. **8** is a cross section of a bipolar device made in accordance with a preferred aspect of the invention.

FIG. **9** is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is described herein with reference to the drawings for both MOS and bipolar applications. FIG. **3** shows an MOS device where P+ drain contact *12a* is formed in P− type drain **12**, P+ source **14** is formed in the N− body **11** and N+ body contact 11_c is provided in the N− body **11**. The MOS channel region 11_b is in the N− body **11** below the MOS gate **16**. The N type top gate **21** is provided along the surface 11_s of the body **11** above the P type drift region **17** which acts as a JFET channel. The lateral edge or peripheral edge of both the top gate **21** and drift region **17** extend to the drain body junction **15** and preferably terminate at the junction **15**. It is noted that situations may exist where the doping level in the top gate may be sufficiently high so as to render it desirable to provide a shorter top gate having a lateral extension which stops short of contacting the junction **15**. In this case care should be taken to insure that any non-depleted portion of the top gate does not result in a breakdown of the top

gate to drift region junction. Proper doping of the top gate will generally be a sufficient preventative step. Dashed line 21_p designates the peripheral edge of top gate 21 in an embodiment where the top gate does not extend all the way to the junction 15.

The structure of FIG. 3 provides reduced ON resistance in the JFET channel relative to the prior art lateral drift MOS device as shown in FIG. 1. The reduction in ON resistance is accomplished by providing a structure which can accommodate increased drift region doping without suffering from reduced body to drain breakdown. This is possible because of the provision of the top gate 21. The top gate to channel depletion layer which holds some channel charge when reverse biased, is in addition to the channel charge held by the bottom gate to channel depletion layer of the prior art. This additional channel charge, in the form of ionized channel impurity atoms, results in the reduction in channel resistance. It is possible to provide more than twice the doping level previously acceptable due to the additional ability to hold channel change. Thus, for a drift region having a doping of 1×10^{12} boron atoms per square centimeter over the drift region surface in a bottom gate arrangement, the present invention will permit 2×10^{12} boron atoms per square centimeter. Thus, the ON resistance will be only half the ON resistance of the prior arrangement.

In order to optimize performance of the structure of the invention, the top gate 21 must be designed differently than an ordinary JFET gate. Top gate 21 should become totally depleted at a body to drain voltage of less than the breakdown voltage of the top gate to drain junction 15_a. Since top gate 21 is connected to body 11, the voltage at the top gate to drain junction 15_a will equal the voltage of the body to drain junction 15 voltage and the top gate to drain breakdown voltage should be greater than the voltage at which top gate 21 becomes totally depleted. Additionally, the top gate 21 should totally deplete before the body 11 to channel 17 depletion layer reaches the top gate 21 to channel 17 depletion layer to thereby assure that a large top gate 17 to drain 12 voltage is not developed by punch-through action from the body 11. An ordinary JFET gate never totally depletes regardless of operating conditions.

In addition to the above described characteristics of the device of the invention, it is also desirable to insure that the channel of the JFET drift region contacts the inversion layer MOS surface channel. This can be accomplished as shown in FIG. 4 where an implant mask 50 having a tapered edge 51 is provided over the body 11. An implant aperture 52 is provided in mask 50 at the location where the P drift region 17 and top gate 21 are to be formed. The aperture 52 is shown as exposing the protective oxide 53. Ion implantation is not substantially effected by the oxide 53 due to the oxide thickness of only about 0.1–0.2 micrometers, yet the oxide provides surface passivation for the underlying body 11.

The drift region 17 is ion implanted and because of the graduated thickness of the implant mask 50 (along the edge 51) the depth of the implanted drift region 17 is graduated or tapered. In the illustration, a fairly good rounding of the drift region 17 occurs at the peripheral edges or extremities 17_a, 17_b of the region 17. The curved extremity 17_a is of interest because at this location the channel of the JFET drift region 17 contacts the surface 11_s of body 11 beyond the end 21_a of top gate 21 and is desirably beneath the gate 16 of the MOS device. The top gate 21 may be ion implanted into the drift region using the implant mask 50 but at an energy level which results in a shallower ion penetration. This tapered profile, particularly if curved, provides improved performance.

In a variation of this method a diffusion process can be used to bring the JFET channel into contact with the surface 11_s of body 11, and hence insure that the JFET channel will contact the inversion layer MOS surface channel. The lateral drift region 17 and top gate 21 are diffused into the body 11 after initial introduction by ion implant. The doping levels and diffusion times are chosen such that the extremity 17_a of drift region 17 diffuses beyond the end 21_a of the top gate 21 and so that the end 17_a reaches the surface 11_s of body 11. In practice, this approach can be facilitated by choosing a top gate dopant which has a lower diffusion coefficient than that of the drift region dopant.

The formation of the drift region and top gate may be conveniently carried out by forming a mask over the gate oxide which is present in a lateral MOS application. The MOS gate may be utilized as one delineating edge of the implant for the drift region and top gate and a thick oxide portion surrounding a thinner oxide portion may form the remainder of the implant mask. The thinner oxide portion shall be located such that it extends from beneath the MOS gate to the drain and preferably overlaps the drain. The implant mask 50 illustrated in FIG. 4 is shown as having thin oxide portion 53 being surrounded by the implant mask 50. If the MOS gate 16 shown in dashed lines were used as a portion of the mask 50, the edge of the drift region and top gate would be self aligned with the MOS gate as shown in dashed lines. Then, when diffused, the drift region will extend laterally to a point beneath the MOS gate while the top gate may be formed such that there is little or no lateral overlap with the MOS gate. The extent of lateral diffusion of the top gate is dependent upon the dopant material and processing temperatures following top gate implant. It is noted that there is a separation between the drift region and the source. This separation zone is the location where the MOS channel is located.

The top gate 21 will perform as previously described if it is tied to the body 11. Thus, the top gate 21 and the body which operates as the bottom gate of the JFET channel will be at equal potential. According to the invention, this may be accomplished in a particularly effective manner if the drift region 17 is widened to overlap with the body contact region 11_c. This is shown in FIG. 5_a which shows the overlapping of the top gate 21 and the body contact 11_c at overlap regions 21_c, 21_d. In order for this arrangement to be effective, it is necessary that the body contact 11_c have a higher dopant concentration than the JFET channel (or drift region) 17 as shown in FIG. 5_b to insure that the body contact 11_c forms a continuous region horizontally and/or vertically through the JFET channel and to the body region 11 from the top gate, 21.

FIG. 5_b shows a cross section of the structure of FIG. 5_a taken along dashed line A—A. The body 11 is provided with body contact 11_c which is located such that the top gate 21 and drift region 17 can be conveniently extended to overlap the body contact 11_c. The depth of body contact 11_c may be made greater than the depth of region 17 such that a portion of the body contact 11_c extends below region 17 and provides contact with the body 11. This arrangement provides a contact portion 21_c where the top gate 21 is in contact with body

contact 11_c. Thus, so long as the body contact doping concentration in region 21_b is sufficiently high to overcome the opposite doping in region 17, then a good connection of uniform conductivity type will be provided between the top gate 21 and the body 11. It is also noted that the body contact 11_c extends laterally beyond the end of both of the top gate 21 and the drift region 17. The lateral extension of the contact 11_c will also provide a structure which results in a good connection of uniform conductivity type from the top gate 21 to the body 11, again, provided that the doping of body contact 11_c converts region 21_b.

Another area where the present invention finds application is in lateral bipolar transistors which employ a lateral drift region. The known structure of FIG. 2 may be improved by providing an N type top gate 126 as shown in FIG. 6. In this arrangement the top gate 126 extends from the collector 124 to the emitter shield 121 along the surface of body 11. The operation of this device is enhanced by the same phenomenon as the lateral drift region of the previously described MOS device. As the base 11 becomes positive relative to the collector 124, the top gate to drift region depletion layer facilitates pinch-off of the drift region. However, as the base 11 becomes more negative the top gate 126 contributes additional surface exposure to the drift region 123 resulting in lower collector resistance.

FIG. 7 shows an improvement over the arrangement shown in FIG. 6. In FIG. 7 the drift region 123 does not extend all the way over to the emitter shield 121. The curved end 123_a of the drift region 123 contacts the top surface of body 11. It is noted that in this arrangement, the emitter shield 121 may be omitted.

An additional improvement shown in FIG. 7 is the use of a deep diffusion to form the collector 124 resulting in a significantly increased breakdown voltage. The deep diffusion step may be the same step used for forming the emitter, in which case the collector 124 shown in FIG. 6 would be deeper, or a separate collector implant and diffusion step may be employed and the collector contact 127 may then be formed simultaneously with the formation of the emitter 122. This improvement in junction breakdown voltage is equally obtainable, for example, at the body to drain junction in the MOS devices described previously.

A further extension of the invention which may be used to increase base to collector breakdown voltage for a PNP device is shown in FIG. 8. In addition to the provision of the N type top gate 126_a over the P− drift region 123_a, the top gate and drift region are enlarged to surround the collector 124 and a curved edge 123_e is provided at the periphery of the enlarged portion 123_b of the drift region. This enlarged portion is designated by reference numerals 123_b for the drift region and 126_b for the top gate. The collector 124 to base 11 breakdown voltage is increased relative to alternative arrangements because of mitigation of the breakdown reduction due to the junction curvature. The top gate 126_a extends to the emitter shield 121 as does the drift region 123_a. The P+ emitter 122 is formed in the N+ type emitter shield.

FIG. 9 illustrates an extension of the invention with respect to a P channel MOS device similar to the improvement described with respect to the bipolar device shown in FIG. 8. For the MOS device, the P+ drain 12 is surrounded by the P− drift region 17 and N type top gate 21. Around the entire periphery of the drift region there is a curved portion 17_e which rounds up to the surface of the N− substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16. The drift region 17 extends outward from the entire perimeter of the drain 12. This arrangement mitigates the breakdown reduction due to junction curvature. The P+ source 14 and N+ body contact 11_c are shown as is the dielectric 13 which serves as the gate oxide 13_g beneath the MOS gate 16.

In both the arrangements shown in FIG. 8 and FIG. 9, the planar diode breakdown improvement created by the drift region acting as a surface layer of the same conductivity type as the collector in FIG. 8 and drain in FIG. 9 and extending out from the perimeter of the collector and drain can be implemented by a single series of process steps. According to the invention, a common set of process steps produces both a suitable breakdown improvement layer and an improved drift region. The breakdown improvement layer is a two layer component.

While the present invention has been described with respect to several preferred manners of implementing the invention, it is to be understood that the claims appended hereto are intended to cover the invention in its broadest sense and are not to be limited to the specific implementations disclosed.

What is claimed is:

1. In a semiconductor device of the type including a lateral drift region of a first conductivity type formed in a body region, said drift region serving as a JFET channel, the improvement comprising:
   - a top gate of a semiconductor material electrically connected to said body region and having a second conductivity type over said drift region to cause depletion of said drift region rom the top upon application of a reverse bias voltage to said device,
   - wherein said top gate laterally abutts a device region to form a junction and has a surface area doping density such that said top gate becomes totally depleted at a reverse bias voltage below the reverse breakdown voltage of the top gate to device region junction, and
   - wherein said top gate has a surface are a doping density such that it becomes totally depleted at a reverse bias voltage less than the reverse bias voltage at which said drift region becomes depleted.

2. A semiconductor device as claim 1 wherein said drift region as a tapered peripheral edge.

3. A semiconductor device as claimed in claim 2 wherein said top gate has a lateral expanse bounded by said drift region.

4. A semiconductor device as claimed in claim 3 wherein said top gate has a tapered peripheral edge.

5. A semicondcutor device comprising:
   - a semiconductor body of a first conductivity type;
   - a first device region of a second conductivity type formed in said body;
   - a second device region of said second conductivity type formed in said body and separated from said first device region;
   - a drift region of said second conductivity type formed in said body between said first and second device regions, separated from said second device region by a separation zone and in contact with said first device region, said drift region having a first side adjacent said body;
   - a top gate of said first conductivity type adjacent a substantial portion of a second side of said drift region and electrically connected to said body;

wherein said top gate and semiconductor body operable as a top and bottom gate respectively of a JFET channel formed by said drift region;

said top gate having a surface area doping density such that it becomes totally depleted at a body to first device region voltage below the voltage at which the body to drift region depletion layer in said first side of said drift region reaches the top gate to drift region depletion layer in said second side of said drift region.

6. A semiconductor device as claimed in claim 5 wherein said first device region is a drain of a lateral drift region MOS device;

said semiconductor device further comprising an MOS gate located over said separation zone and overlapping a portion of said drift region.

7. A semiconductor device as claimed in claim 5 wherein said first device region is a collector of a lateral bipolar transistor and wherein said separation zone comprises an emitter shield region of said first conductivity type.

8. A semiconductor device as claimed in claim 5 wherein said drift region and top gate are in contact with said first device region about the entire periphery of said first device region.

9. A lateral MOS structure comprising a semiconductor body of a first conductivity type, source and drain regions of a second conductivity type forming respective source and drain junctions with said body, and a drift region of said second conductivity type, said drift region forming a JFET channel in said body controlled by said semiconductor body which body operates as a JFET gate such that upon application of a reverse bias to said body to drain junction said drift regions becomes depleted, and

a top gate of said first conductivity type formed in said drift region and being electrically connected to said body, said top gate having a surface area doping density such that it becomes totally depleted below a body to drain voltage at which said drift region becomes depleted.

10. A lateral MOS structure as claimed in claim 9 wherein:

said top gate is laterally spaced from said drain.

11. A lateral MOS structure as claimed in claim 9 wherein:

a body contact of said first conductivity type is formed in said body and said top gate overlaps said body contact, said body contact having an impurity concentration higher than the impurity concentration of said drift region.

12. A lateral MOS structure as claimed in claim 9 wherein:

said drift region and said top gate extend laterally around the entire surface intersection of the drain to body junction to reduce the surface field and thereby increase breakdown voltage of the drain to body junction.

13. A lateral MOS structure as claimed in claim 9 wherein:

said top gate totally depletes below a body to drain voltage at which said drift region totally depletes.

14. A lateral MOS structure as claimed in claim 9 wherein:

said top gate is formed by an ion implant, and said top gate has a tapered peripheral edge.

15. A lateral MOS structure as claimed in claim 14 wherein:

said drift region is formed by an ion implant and said drift region has a tapered peripheral edge.

16. A diode structure comprising:

a first semiconductor body of a first conductivity type contained within a semiconductor region of a second conductivity type and forming a diode junction therewith, said semiconductor region having a first dopant concentration,

a second body of said first conductivity type contained within said semiconductor region and having a second dopant concentration greater than said first dopant concentration, said second body surrounding the lateral perimeter of said first body and abutting said first body;

said second body forming a JFET channel controlled by said semiconductor region which region operates as a JFET gate such that upon application of a reverse bias to said region to first body junction said second body becomes depleted, and

a top gate of said second conductivity type formed within said second body and being electrically connected to said first semiconductor region, said top gate having a dopant concentration such that upon application of said reverse bias, said top gate becomes totally depleted before said second body becomes depleted.

17. In a diode structure as claimed in claim 16, the improvement comprising:

a tapered peripheral edge for said top gate.

18. In a diode structure as claimed in claim 17, the improvement comprising:

forming said tapered peripheral edge by implanting said top gate using an implant mask with a tapered edge.

19. In a diode structure as claimed in claim 16, the improvement comprising:

forming a tapered peripheral edge for said second body by implanting said second body using an implant mask with a tapered edge.

* * * * *

EXHIBITS 10 – 35

REDACTED IN THEIR ENTIRETY

CERTIFICATE OF SERVICE

I hereby certify that on the 1st day of December, 2006, the attached **REDACTED PUBLIC VERSION OF DECLARATION OF GABRIEL M. RAMSEY IN SUPPORT OF FAIRCHILD'S SUPPLEMENTAL BRIEF IN SUPPORT OF DEFENDANTS' REQUEST TO USE ELEVEN PRIOR ART REFERENCES DURING THE INVALIDITY PHASE OF TRIAL** was served upon the below-named counsel of record at the address and in the manner indicated:

William J. Marsden, Jr., Esquire — HAND DELIVERY
Fish & Richardson, P.C.
919 N. Market Street, Suite 1100
Wilmington, DE 19801

Frank E. Scherkenbach, Esquire — VIA FEDERAL EXPRESS
Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804

Howard G. Pollack, Esquire — VIA FEDERAL EXPRESS
Fish & Richardson P.C.
500 Arguello Street, Suite 500
Redwood City, CA 94063

/s/ Lauren E. Maguire

Lauren E. Maguire